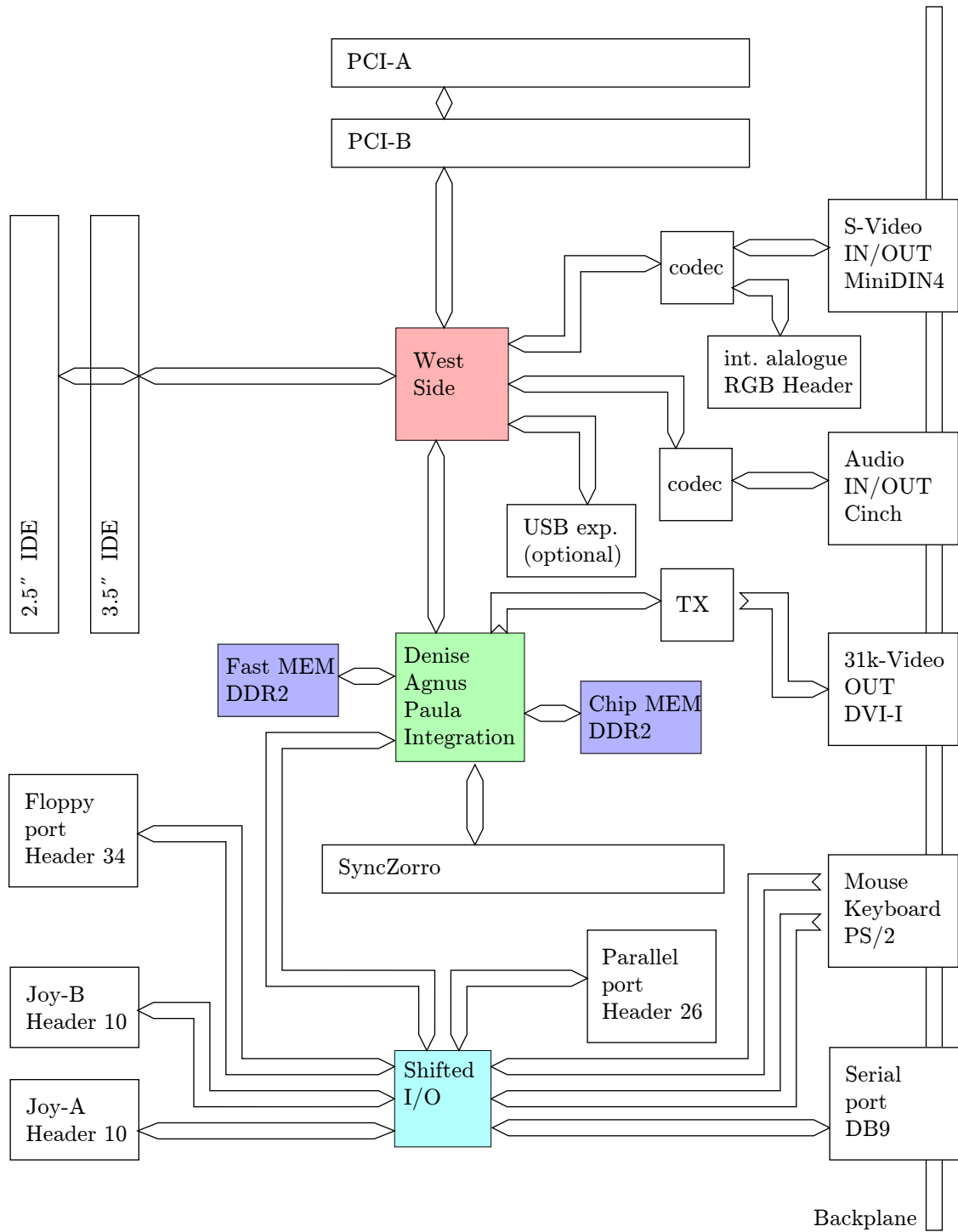


I. Block Diagram



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"West Side" is a fully 3.3V FPGA (or CPLD - depends on the point of view) and attached to the green FPGA via an internal communication bus. It manages the fast RAM DMA connections to the IDE and PCI ports. Two PCI connectors are on board a third one might be accessible through a riser card. This chip will also handle the "slow" (15kHz) video ports and audio I/O. Audio input is a standard 16bit stereo ADC from cirrus logic. In contrast to the audio output which is a modified operational amplifier stage similar to the classic Amiga. It works like bitstream technology but is completely untested. But in theory the resulting sound should be much better with this solution than with a fixed sample rate DAC. The big advantage will be that there is not a fixed sample rate which would surely limit the sound quality because the chipset is built to play different samples with a different period (-> sample rate) at a different time.

The "Shifted I/O" chip is another CPLD which holds all slow peripheral I/O pins and is 3.3V whereas the green FPGA is mostly 1.8V. It is attached by only four wires and therefore the data will be shifted in serial order in both directions.

The green FPGA will hold the core logic including chipset, display generation, CIAs, memory and SyncZorro interface.

All connectors will be internal headers, except:

- 15k Video in- and output: stacked MiniDIN 4
- Audio in- and output: Cinch
- 31k Video output: DVI-I
- Mouse and Keyboard: stacked MiniDIN 6
- Serial port: DB9